TECHNICAL PAPER

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

# INDIUM BUMP INTERCONNECT (IBI) FLIP CHIP BONDING

***Abstract*** *– Focal Plane Array (FPA) imaging and detector devices such as infrared (IR) thermal imaging sensors, Quantum computing processors and micro LED displays are seeing higher demand as more practical applications requiring these components are coming into research and development, military, industrial and consumer markets. This paired with higher pixel and Qubit count and interconnect density on larger and larger chips is driving hybridization and monolithic integration in these technologies. This is showing a marked increase in demand for fine pitch micro Indium Bump Interconnect (IBI) flip chip die bonding. However, some critical challenges facing these technologies are: larger component sizes mean higher density interconnections over increasing surface area. Sub-micron accuracy is required to align fine pitch micro interconnect arrays. This together with the challenges facing the materials that are becoming the industry standard for these applications, such as the requirement for the assembled components to remain stable in extreme conditions such as cryogenic application environments, combined with low loss high strength mechanical / electrical interconnect requirements on components containing sensitive materials, structures and unmatched coefficient of thermal expansion (CTE) means that processing gases such as formic acid or high temperature reflow bonding can no longer be used to bond these devices. These challenges mean that the industry is fast approaching the limitations of even state-of-the-art die bonders and die bonding methods on the market today. This paper is going to highlight these challenges and the methods used to address them to produce large format, high density Infrared (IR) thermal imaging devices, Quantum processors and micro LED displays using fine pitch micro Indium Bump Interconnections (IBI) that meet today's industry requirements.*

## I. Introduction

This paper will address the challenges and solutions faced in Indium Bump Interconnect (IBI) applications. Indium bump Interconnection (IBI) is used in many applications such as Infrared (IR) Thermal imaging devices, Quantum processors, micro LED displays and X-Ray detectors to name a few examples. As Infrared (IR) thermal imaging devices are one of the most challenging applications in this list and the methods used to address the challenges faced while bonding them overlap all other applications, listed above, this paper will focus on IR thermal imaging devices as the main example application.

The application material of Indium Bump Interconnect (IBI) flip chip bonding, such as Infrared (IR) thermal imaging focal plane arrays (FPA), quantum computer processors, X-Ray detectors and micro LED displays covered by this paper usually consists of one or more components or chips bonded to a substrate using a fine pitch array of vacuum deposited micro Indium bumps.

There are many challenges involved in bringing these components together to form a fully

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

functional assembly, such as co-planarity, accuracy, interconnect yield, mechanical/electrical strength and interconnect quality while maintaining a competitive yield and throughput in the respective industry.

To ensure a highly repeatable high yield flip-chip bonding process that meets these requirements, a number of solutions have been developed and tested to address these challenges. As well as addressing tertiary issues, such as tweezer safe handling, cleaning, kitting and loading of the material as well as reducing oxides and organic materials on the Indium bumps or under bump metallization (UBM) pad interconnect surfaces, to reduce the time required to prepare the material for bonding and reduce the risk of yield drop or damaging the material via manual handling.

## II. Indium Bump Interconnect Flip Chip Die Bonding

### Die bonding process

The die bonding process of IR thermal imaging sensors can range from a higher force cold compression bonding process to thermal compression bonding and onto to formic acid reflow bonding, depending on the final application environments and quality requirements.

Due to the high cost of the application materials of Infrared (IR) Focal Plane Arrays (FPA) and their Read Out Integrated Circuit (ROIC) components as well as the time and difficulty involved to produce high quality functional material, it is vital that the initial bonding trials can produce successful parts with minimal trial and error or bonding failure while maintain this high yield moving into the production stage.

The following will outline the processes and preparations as well as software, hardware and process solutions used to achieve and exceed industry requirements for flip chip die bonding of high resolution thermal imaging sensors.

### Material preparation and handling

Compression die bonding of fine pitch micro indium bump interconnect arrays consists of one or more components and a substrate. In this paper we will use the example of a single Infrared thermal imaging sensor (IR Sensor) and Substrate (ROIC) both containing an interconnect layer of fine pitch micro Indium bump interconnect arrays (Indium bump to bump bonding), as this is the example with the smallest bumps and smallest bump array pitch over the largest surface area, making it one of the more challenging applications to address.

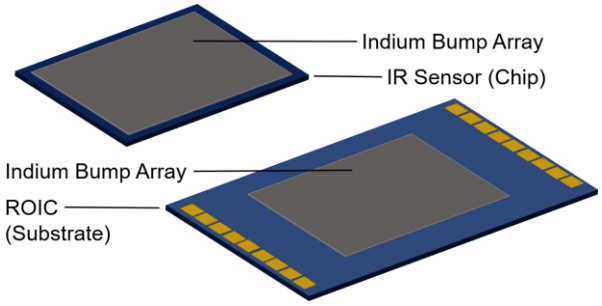


**Figure 1.** IR Thermal imaging FPA and ROIC components

**Figure 2.** ⌀5 µm bump, 15 µm pitch Indium bump array

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Travis Scott, Finetech

Contact:
techpaper@finetech.de

## Material

The fine pitch micro Indium bump array is usually grown on the component and/or substrate material using an Indium vacuum-evaporation deposition process onto the UBM on a substrate covered by a photolithography exposed mask of photoresist, after the bump array has been grown on the wafer, the deposition mask is removed, and in some cases a fresh layer of photoresist is deposited to protect the delicate indium bumps from physical damage, prevent oxidisation and prolong the shelf life of the material. [2]

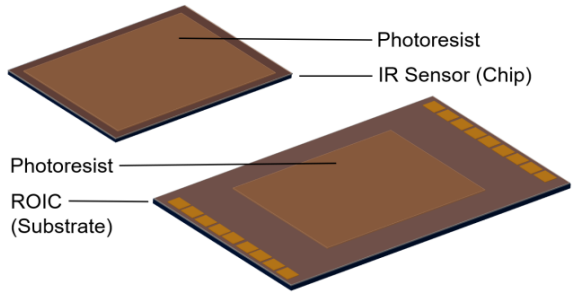


**Figure 3.** Photoresist-coated components

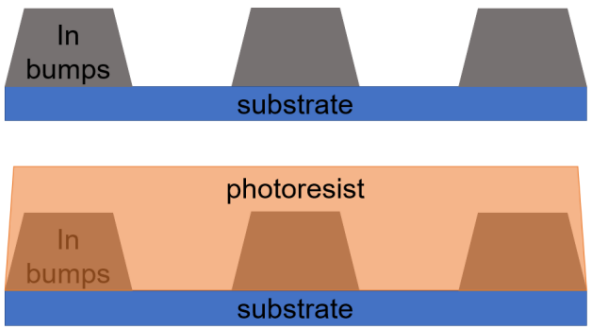


**Figure 4.** Open [top] and Photoresist-coated [bottom] Indium bumps

## Preparation

The first challenge most encounter when preparing to bond fine pitch micro indium bump arrays, is the removal of the protective photoresist layer and the cleaning and removal of all contamination and particles (Particles > 1.0 µm) from the Indium bump array area. To address this challenge a standardized chemical cleaning and material kitting process, to prepare material packs for automated bonding of multiple assemblies with minimal handling of the components to reduce risk of contamination or damage was developed. A material cleaning and kitting module was developed to allow for seamless safe material handling while drastically reducing the use of tweezers and number of handling steps in the handling, loading/unloading and inspection of the material.

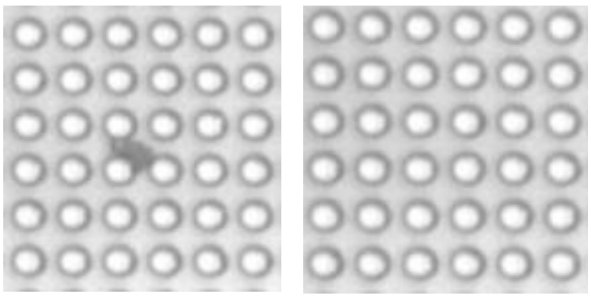

**Figure 5.** ~10 µm contamination removed between Indium bumps

## Handling

Handling of the material during the cleaning, kitting and loading/unloading of the material to die bonder, as well as post bond inspection processes, poses the greatest risk of damaging or contaminating the components and more critically the Indium bump array. To address this challenge a material handling, kitting and loading system that reduces the requirement of tweezer handling to only the initial step of loading the materials into a kitting try was developed. Once the components have been loaded into the handling trays they can be easily inspected,

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Travis Scott, Finetech

Contact:
techpaper@finetech.de

flipped and loaded to be presented both “Indium up” or “Indium down” into the die bonder for the automated die bonding process, after bonding the assemblies can be removed and transferred to post bond analysis procedures all without the use of tweezers. This method significantly reduced the occurrence of particle contamination while reducing the chance of damaging the indium bump array or dropping the components. This method has reduced the material preparation and bonding time in application by more than 50%. The module allows for enough material of at least 4-6 assemblies of 640x512 to be loaded and then bonded with no operator interaction required, which is a significant improvement in throughput and risk reduction.

All materials of the handling pack can aggressively be cleaned with acetone without risk of generating particles or contamination. The functional elements of the kit can also withstand high compression bond forces, high reflow bond temperatures and formic acid process gas and plasma cleaning meaning that it is suitable for both cold compression bonding or formic acid reflow bonding processes.

All clamping and work holding is supplied by vacuum and the pockets can be defined to either avoid all contact with the Indium bump array and sensitive areas on the components or limiting the “fall gap” of the component during flipping to <500 µm ensuring that the maximum force exerted on the Indium bump array would only be the weight of the component itself.

**Tooling requirements**

The tooling required to carry out the automated die bonding of fine pitch micro indium bump arrays will be broken down into tooling for the die handling and tooling for the substrate handling, but the mechanical requirements for both chip and substrate handling and their contact/bonding surfaces are very similar.

**Material and Flatness**

The materials and as the flatness of the tooling and bonding surfaces required to withstand high force and high temperature bonding environments with corrosive processing gases/vapors such as formic acid were a critical consideration during this project.

As the technology for fine pitch micro Indium bump growth/deposition develops, the tendency is for the interconnect size and pitch to decrease as the overall interconnect density increases, meaning that bump height and diameter is steadily heading into the ranges of single microns and potentially sub-micron bumps or interconnects on similar or larger sized components in the near future.

In the more extreme case of IR FPAs show a trend towards component sizes up to 20 - 50 mm, coated almost completely in Indium bump arrays of ~5-7 µm bumps at a 15 µm pitch, with only the ROIC or FPA component containing Indium bumps and the other only metallised pads, leaving only 2-4 µm bond line thickness across the bond.

Due to this, one of the main requirements of the component handling and die bonding surfaces is flatness. In these extreme cases bonding surfaces need to meet flatness requirements below 0.5 µm over a surface area larger than the components themselves (< 0.5 µm over 20mm for example).

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

There are a range of solutions to solve the flatness requirement. These range from precision lapped and polished surfaces, compound tools made of two or more components/materials and speciality materials for the bonding interface surfaces depending on the chosen process. For the reflow and formic acid processes, materials such as Copper Tungsten (WCu) were evaluated for more stable coefficient of thermal expansion (CTE) and efficient heat transfer, composite Tungsten (W) tools were tested for cold compression bonding to preserve flatness.

**Vacuum structure**

A bonding impression is when the resulting image of a sensor has a “ghost” pattern or regular pattern breaking the uniform image of the sensor. This is usually caused by non-uniform force distributed across the bonding surface.

A common example of this in sensor bonding is the shape of the vacuum structure, used to hold the component on the bond tool, being transferred and seen in the final output image of the sensor as a result of less force being applied in the gap between tool and component left by the vacuum structure.

Larger vacuum channels can also deform and bend the chip itself into the vacuum channel if the chip is thin enough and the vacuum structure is too wide.

To mitigate this phenomenon, tooling and work holding were all defined with the narrowest and smallest vacuum structures possible, depending on the tool material and component size. This thinner vacuum structure also showed improved surface flatness specifically around the vacuum structures.

**Automated die bonder requirements**

The die bonder requirements outlined here are required for the automated production bonding of standard format IR sensors from 640x512 up to 2 Megapixel imaging sensors containing 5 µm Indium bumps at 15 µm pitch.

- Post bond accuracy < 0.5 µm @ 3 sigma with a CpK of 1.67
- Automatic calibration of the die bonder is required to maintain post bond accuracy over multiple days and high temperature duty cycles within the die bonder
- Controlled handling and accurate fine force control during touching down to components as well as the initial touchdown and force control during the bonding process is critical to maintain post bond accuracy, to mitigate sliding or shearing during the bonding process and to prevent damage or coining of the Indium bump array.

**Bond process parameters**

Bond force

- Low forces are required to mitigate damage to the delicate indium bumps. Low forces used in 640x512 component handling in the die bonder in the range of 0.05 N – 1.0 N showed no visible change to the bump surfaces when picking up or placing to a flat clean surface.

- Fine control of force ramps in the bonding profile were desired to ensure no slipping or shearing occurred during force build up. Up to 1.0 N/s was used and showed stable results, however

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

faster ramp rates could deliver similar high yield results.

- A typical cold compression bonding force of 20 N/mm$^2$ [4] of indium bump area will result in an estimated 50% compression of the total bump height of two components containing a vacuum deposited Indium bump array.

Bond profile

The temperature profile depends on the chosen bonding method. Thermal compression and reflow bonding processes will require reduced forces.

- Cold compression Bonding = room temperature up to 90°C
- Thermal Compression Bonding = 100 to 164°C
- Reflow Bonding = 165°C +
- Formic acid reflow bonding = ~210°C oxide reduction / 165°C+ reflow

**Modules**

The automated FINEPLACER® die bonder systems can fitted with a variety of modules the following modules to specifically address Indium bump interconnect bonding challenges. Each module aims to address a specific challenge faced when carrying out cold, reflow and formic acid reflow flip chip bonding of fine pitch micro Indium bumps.

- **Heated Modules**

For thermal compression bonding, reflow bonding and formic acid reflow bonding processes the bonding surfaces of the bond head and substrate carrier may be required to reach the elevated temperatures required to melt and reflow the Indium bumps (165°C +) as well as reaching the activation temperature required to reduce the oxide layer found on the Indium using formic acid (~ 210°C).

- **Tool Tip Changer Module**

To allow multiple tools to be used in a bonding process the tool tip module was used. Allowing the automated loading and unloading of operation specific tools, for example, and the automated camera calibration could be carried out using the calibration tool and then the bonder could immediately proceed to the automated Indium bonding process.

This was useful specifically during the high temperature duty cycle processes. To maintain very high accuracy.

- **Tool Levelling Station for co-planarity**

Due to the height of the micro Indium bump array as well as the large component size, co-planarity is vital to the bonding process, to allow for even pressure and a parallel, even bond line across the entire bump array.

To compensate and correct the co-planarity of the tooling, a passive levelling method is used that can correct tool co-planarity to within < 0.5 µm over a 25 mm tool surface.

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

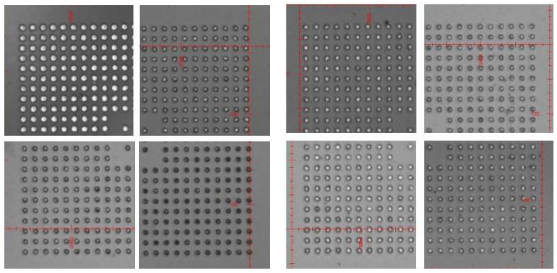

**Figure 6.** [left] ~ 5 µm co-planarity error (more compression on the top left, no contact bottom right). [right] < 1 µm co-planarity error (even compression over the full 10 mm² area)

- **Inert Gas / Formic Acid**

For reflow and formic acid reflow bonding processes the bonding area was supplied with an inert gas to create an inert environment using Nitrogen (N2), or a processing gas such as Formic acid vapor to reduce oxides on metal surfaces to expose fresh Indium bonding surfaces.

To reduce oxide on the Indium bumps or to reform the pyramid shaped bumps into more uniform and less amorphous spheres the Indium can be reflowed in a formic acid environment with a laminar flow to carry away the oxides.

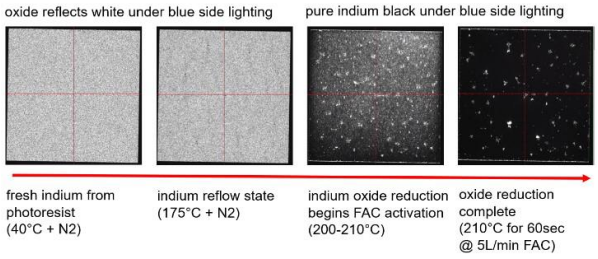


**Figure 7.** Indium oxide reduction under FAC process gas

Once formic acid reflow is complete the components can be observed to contain far less oxide, with a majority of the surface being pure Indium or a very thin layer of oxide covering the Indium making for a higher strength and higher electrical quality bond surface.

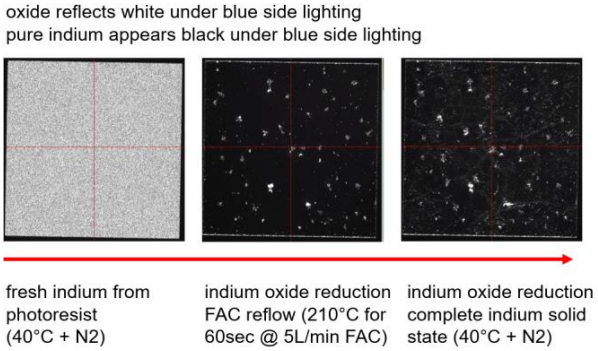


**Figure 8.** Indium oxide reduction under FAC and cooled to solid state under N2

- **Laser Height Measurement**

The automated FINEPLACER® system used for bonding is fitted with a Laser Height Sensor Module for various measurement, evaluation and qualification functions.

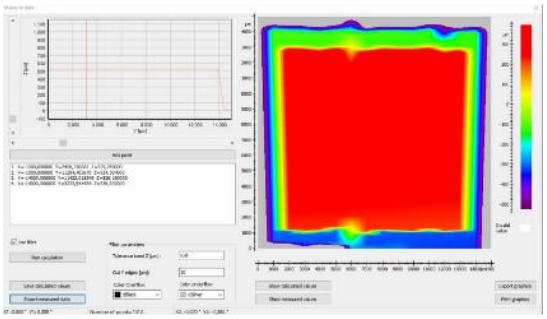

**Figure 9.** Laser height measurement (Surface Height Measurement)

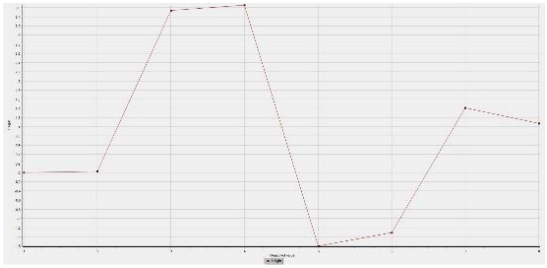

**Figure 10.** Laser height measurement (Point Height Measurement)

The module can be used to measure and evaluate tool surfaces, bonding surfaces and component

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

surfaces for flatness as well as co-planarity. The module can be used to estimate the height between the top surface of the substrate and component for bond line thickness (BLT) using 3 or more points in a point height measurement process. A more detailed line scanning process (pictured above) can be used to generate a topographical map of the surface being measured with a sub-micron resolution.

This allows for an in-situ analysis and evaluation of the bonded assemblies for flatness, co-planarity and estimating the bond line thickness without having to transfer them to another equipment.

## III. Results

### Flatness and co-planarity

Optimizing the hardware and tooling design, in addition to the passive levelling of the tools enabled consistent, repeatable and controllable flatness and co-planarity in the bonds.

The flatness and co-planarity achieved on the 5 µm bump, 15 µm pitch 8x10 mm$^2$ 640x512 IR FPA trials was consistently below 1 µm.

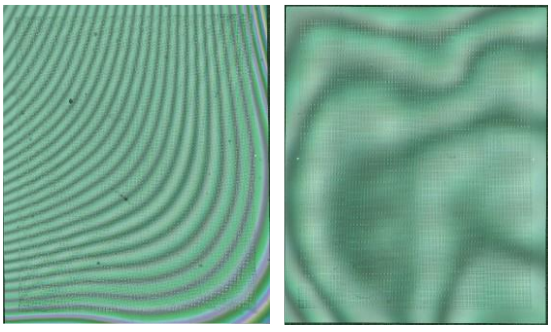

**Figure 11.** [left] ~ 5-6 µm co-planarity error**.** [right] ~ 1 µm co-planarity error

(Newton ring effect, each 4 lines is estimated to be ~ 1 µm. Observed through transparent component, 130 N over 5 µm bump, 15 µm pitch 640x512 Indium bump array).

### Accuracy

To develop the tooling requirements, bonding process and fine tune the bonding parameters a transparent chip with indium bump array was bonded to an ROIC with indium bump array. This trial was also used to assces post bond accuracy.

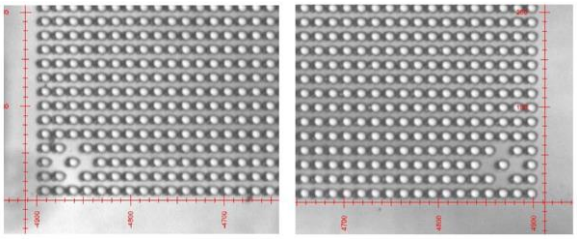

**Figure 12.** ~ 4-5 µm offset error (during early trials with flatness and co-planarity issues during bonding)

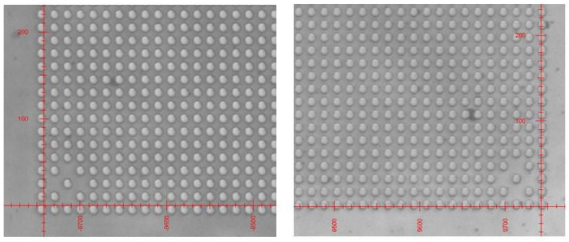

**Figure 13.** < 1 µm offset error_ observed through transparent component 130 N over a 640x512 format _ 5 µm bump, 15 µm pitch 10x8 mm$^2$ Indium bump array.

By optimizing the tooling, cleaning, process preparation and bonding parameters in combination with automated camera calibration processes, it was possible to consistently bond the components within 1 µm over many trials per day and maintain this quality over extended periods of time (1–2 weeks) without having to adjust the system.

Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

**Interconnect Quality**

Real IR FPAs were bonded using these methods and underwent functional testing and stress testing for operation in cryogenic environments. Unfortunately these results cannot be shared but the results showed and interconnection yield of above 99% of the components with good dark current characteristics while withstanding high stress duty and temperature cycles.

## IV. Discussion

**Indium Bump Interconnect**

Indium bump arrays are seeing larger adoption in quantum computing with very demanding requirements for co-planarity and control of bond line thickness as well as high quality electrical interconnections, IR FPAs are showing a constant drive for higher resolution meaning smaller bumps, higher density, and larger surface areas, and finally the higher consumer market demand for µLEDs or Micro LEDs means that much higher through put will be required for fine pitch Indium interconnects.

These requirements will become quite demanding for the die bonders on the market today and will drive further innovation to solve these challenges in novel ways.

With the introduction of Cu-Cu wafer level bonding, to mass produce SWIR image sensors [3], the pressure to reduce costs of manufacturing Indium interconnect IR thermal imaging devices will also drive development and push for further automation in this market to reduce the cost per bond.

## V. Conclusion

Fine pitch micro Indium bump interconnect bonding is a challenging application, however using the methods described above it is possible to take this challenging bonding process and streamline it into a more stable low volume production process, removing risk of damage or failure while improving yield and bond quality in a more controllable and repeatable manner over sustained automated production cycles.

The FINEPLACER® femto 2 automated die bonder including the tooling and modules in combination with the improved cleaning and handling methods developed for this process, is an Ideal solution for low level production or research & development of any fine pitch micro Indium bump interconnect application for IR FPAs, quantum computing processors, X-Ray detectors or µLED displays for example.

## VI. References

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Author:
Travis Scott, Finetech

Contact:
techpaper@finetech.de

**Company Profile**

Finetech is a leading equipment manufacturer for sub-micron die bonding and advanced die packaging. Along with manual and semi-automated die bonder systems for quick product development, the company offers micro assembly platforms for fully automated production.

Finetech helps technology start-ups and industry leaders worldwide to develop and manufacture innovative semiconductor products. Served customers are companies e.g. in the fields of Datacom & Telecom, Industrial Semiconductor, Medical Technology & Life Sciences, Aerospace & Avionics, Automotive & Transportation, Defense & Security, Consumer Electronics, and Academic & Scientific Research.

The modular hardware and software architecture of Finetech's die bonder systems allows application-specific machine configurations. New processes and technologies can be added via extension modules at any time to ensure optimal process environments for each type of application. Finetech's cross-system "Prototype-to-Production" approach with a unified module and software platform allows thinking ahead all automation steps as early as the process development stage. This ensures a streamlined transfer of developed processes in all their technological diversity to the production stage and makes Finetech equipment the perfect fit for flexible and cost-efficient product development.

Supported bonding technologies include eutectic soldering, adhesive bonding, thermocompression bonding, thermo-/ultrasonic bonding, sintering, laser-assisted bonding and precision vacuum die bonding. Die bonders by Finetech are used for the precision assembly of flip-chips, photonics and opto-electronics, as well as all kinds of high I/O count applications at chip and wafer level.

Finetech responds flexibly to specific requirements and offers tailor-made solutions to highly demanding customer applications. The company is represented by direct subsidiaries in its core markets and offers on-site application support and advice. It is also represented world-wide by a network of agencies.

Finetech is headquartered in Berlin, Germany, with subsidiaries in the USA, China, Thailand, and Japan.